Features

- LDPC encoder for 5G and WiFi (802.11n, 802.11ac, 802.11ax).
- Automatic insertion of shortening bits, puncturing of parity bits and generation of repetition bits. In 5G mode the output may be offset to a starting position for incremental redundancy.
- Multi-user contexts.
- Simple software control – configured once at the start of the packet.
- Very high speed encode rate. Z bits are encoded in parallel.
- Configurable IO bit-widths.
- Total encode times of 641/494 cycles for BG1 and BG2 respectively, giving more than 10Gbps data throughput for the highest 5G code rate assuming double buffered memory.
- 5G LDPC block-level CRC insertion before encoding and output of coded data in interleaved order.
- Efficient hardware architecture. Approximately 100K ASIC gates and 26112 bits of single port RAM.

Deliverables

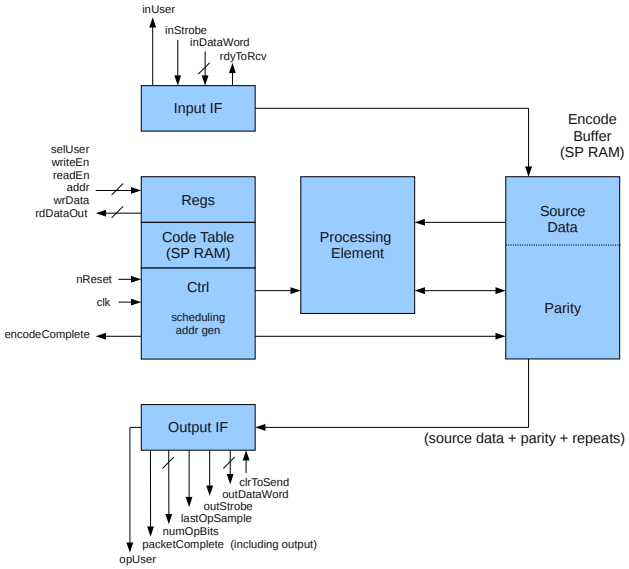
- RTL (VHDL|Verilog5G) block description and test harness with test vector files.
- C model.
- User and Hardware Integration Guides.

General Description

This product provides low latency, high throughput encoding of 5G or 802.11n/ac/ax packets. Configuration by software is only required once per packet. The block autonomously loads a block of input data, encodes it and then delivers it to downstream hardware.

A small memory stores data, while a single, high bandwidth, processing element (PE) performs the necessary syndrome and parity generation, stepping through each code 'macro cell' at a rate of around 2 cycles per cell.

Block Diagram



The encode time is extremely low and IO overheads can dominate the overall latency. This can be mitigated by configuring for high throughput, or by using a double buffered configuration.

Implementation Notes

The single buffered configuration uses one buffer to perform input->encode->decode, consequently encoding is only possible for a portion of the time.

The double buffered configuration passes a buffer containing one LDPC block from input → encode → output, while a second buffer processes the next block in the same sequence. As each of the processing stages (input, encode and output) completes the processing of one block it switches to the next block resident in the other buffer. When the IO bandwidth is sufficient to allow input and output in less time than it takes to encode a block, 100% encoder utilization is achieved.

As a rough guide, an ASIC implementation of this IP is estimated to contain around 100K gates of logic (full 5G version) and one or two RAM instances totalling of 26112 bits each. The RAM is single port and write-maskable features are required (or are emulated by separating the encoder RAM into several slices).

Licence

The licence is tiered to allow migration from a development licence to single or multiple use manufacturing licences. Support and Maintenance will be provided for 12 months in the form of clarifications about the product and bug-fixing as well as design enhancements.

The licence provides access to the technical information of the product and does not imply a licence from parties that may claim ownership of the technology, for example through patents. You will certainly need to investigate *Essential IPR* licensing requirements before making a product.

Full terms and conditions are provided with formal quotations.

Warranty

This deliverable provides a 5G multi-stream LDPC encoder and 802.11n/ac/ax multi-stream LDPC encoder. It may be practically implemented on an FPGA or ASIC assuming high performance parts or processes. Naturally the performance of the decoder will be determined by your choice of process, clock speed and system level throughput.

Product Selector

The following table shows this product (highlighted with *) alongside related products. Click the PDF icon to view the datasheets. The simplest product choice is to take only the RTL, however if you wish additional flexibility and the rights to modify the design then you can take the algorithm product as well.

Code	Description	
LDPCDEC5GR	5G/WiFi LDPC Decoder	email
LDPCDEC11APR	802.11n/ac/ax Access point multi-user/core LDPC Decoder	email
LDPCENC11NR*	802.11n/ac LDPC Encoder RTL IP	
LDPCDEC11NR	802.11n/ac LDPC Decoder RTL IP	
LDPCENCADR	802.11ad LDPC Encoder RTL IP	
LDPCDECADR	802.11ad LDPC Decoder RTL IP	
VITDEC11NR	802.11n/ac Viterbi Decoder RTL IP	

About Blue Rum Consulting

Blue Rum Consulting is a UK limited company offering the services and products of Michael Rumsey, a Wireless ASIC engineer with more than 30 years of experience. You can find him on linked-in and the company web-site at www.bluerum.co.uk