Features

- LDPC decoder for 802.11ad supporting all code rates (1/2, 5/8, 3/4, 13/16) using the 672 bit code word defined by the 802.11ad standard.
- Supports all MCS (the highest, MCS 24, being 6.756 Gbps).
- A range of architectural options allow reduced gate-count where lower data-rates are acceptable.
- Implementation losses of around 0.3dB compared to a 50 iteration floating point reference.

Deliverables

- RTL (VHDL) block description and test harness with test vector files.
- C model and Octave/Matlab sim environment for generation of performance data and RTL verification vectors.
- Performance (BLER/BER/PER) data.
- User Guide.

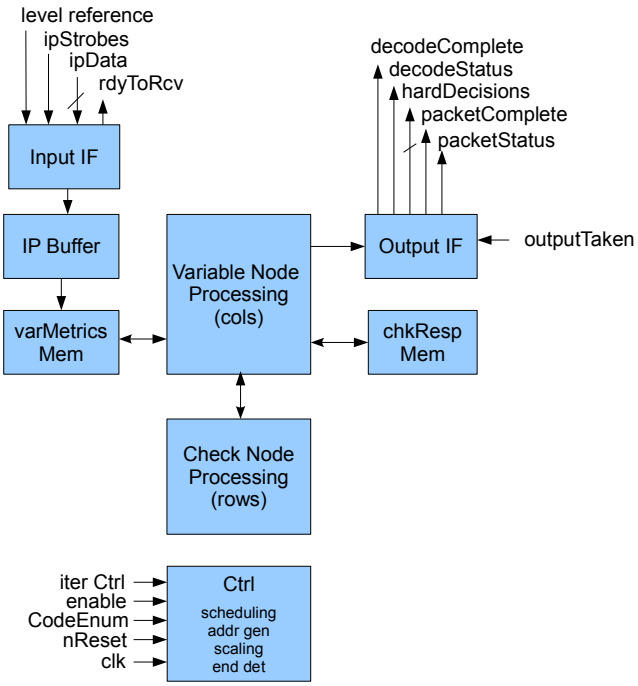
General Description

The LDPC decoder stores samples (LLRs) from the preceeding block - typically a QAM demapper - in a buffer. The number of samples input per cycle is configurable. The buffer is fetched into the 'variable node' processing unit as soon as the processing unit has completed any previous block. The decoding iterations then begin.

Each decode iteration takes 1-4 clock cycles depending on the selected architecture. Typically there are 3 or 4 iterations but occasionally significantly more are required.

End condition detection is based on parity checking and gated-clocks are used to save power if the decoder has to wait for the next block. 672*R (R being the code rate) output hard-decisions are provided on a 546 bit output bus to allow you the flexibility of optimising your integration.

Block Diagram



Interface

The code for the decoder is defined at synthesis time. Consequently various tuning parameters are also be hard-coded so there is no need for a processor interface. This makes the interface particularly simple:

- LLR input with level reference. The width (number of samples per cycle) is configurable.
- Enable.
- Code Rate select.
- Direct 672*R bit output.
- Decode complete strobe and status.
- Packet complete strobe and status.
- Optional iteration control (defaults will be used if this is tied to zero).
- Optional packet length input.
- Additional outputs to facilitate test benches.

Performance

We characterise the performance of the key MCS cases with the most appropriate of the architectural options. Typical implementation losses are around 0.3dB, which includes losses due to the following:

1. Finite precision arithmetic. The recommended configuration results in approximately a 0.1dB loss.
2. The corrected min-sum approximation. This performs to approximately 0.1dB of the true mathematics that uses exponentials. Note that the un-corrected min-sum approximation would have resulted in a loss of greater than 0.5dB.
3. Limited number of iterations.

For more formal performance data please ask for the detailed specification, which provides detailed performance measurements, and area and power estimates.

Customisation

The decoder design is flexible and has the potential (subject to contract) to be adapted for applications other than 802.11ad. 802.15.3c is a closely related standard for which we could provide support. Likewise the decoder may suit the requirements of Hard Disk Drive Manufacturers. Please contact us with your requirements.

Licence

The licence is tiered to allow migration from a development licence to single or multiple use manufacturing licences. Support and Maintenance will be provided for 12 months in the form of clarifications about the product and bug-fixing as well as design enhancements.

The licence provides access to the technical information of the product and does not imply a licence from parties that may claim ownership of the technology, for example through patents. You will certainly need to investigate *Essential IPR* licensing requirements before making an 802.11ad product.

Full terms and conditions are provided with formal quotations.

Warranty

This deliverable provides an 802.11ad LDPC decoder that may be practically implemented on an FPGA or ASIC assuming high performance parts or processes. Any functional or performance defects preventing 802.11ad qualification will be resolved inside and outside of the maintenance period.

Product Selector

The following table shows this product (highlighted with *) alongside related products. Click the PDF icon to view the datasheets.

Code	Description	
LDPCENC11NR	802.11n/ac LDPC Encoder RTL IP	
LDPCDEC11NR	802.11n/ac LDPC Decoder RTL IP	
LDPCENCADR	802.11ad LDPC Encoder RTL IP	
LDPCDECADR*	802.11ad LDPC Decoder RTL IP	
VITDEC11NR	802.11n/ac Viterbi Decoder RTL IP	
AESCRYPTO	AES Cryptography with CCM, and (optionally) CMAC and GCM.	

About Blue Rum Consulting

Blue Rum Consulting is a UK limited company offering the services and products of Michael Rumsey, a Wireless ASIC engineer with 30 years of experience. You can find him on linked-in and the company web-site at www.bluerum.co.uk .